REMARKS

Applicant thanks the Examiner for indication of allowable subject matter in claims 9-16, and for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Applicant notes that the priority document was received in the parent to this application, US Patent Application Serial No. 10/435,416.

Responsive to the Office Action mailed on August 24, 2004 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-16 are pending in the application. Claims 17-22 are cancelled. Claims 1-8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al (US 6,534,915). Claims 9-16 are allowed.

In this paper, new claim 23 reciting that the floating gate consists of the conducting layer and the conducting spacer is added. Support for the new claim can be found in the original claims and on page 7, lines 17-20 and Fig. 2H. Claims 1 and 9 are amended to improve grammar. The specification is amended to correspond with the amended claims and correct a typographical error. Figs. 2a, 2g and 2h are amended to correct typographical errors and more accurately reflect the steps of the process described on page 7 of the specification.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Drawings

Fig. 2a is amended to correct a typographical error therein. Namely, after amendment, the opening 206 is correctly identified as such. Figs. 2g and 2h are amended to more accurately reflect the steps of the process described on page 7 of the specification.

AMENDMENTS TO THE DRAWINGS

The attached two (2) sheets of drawings include changes to Figures 2a, 2g and 2h. Replacement Sheet 1 replaces the original sheet for Figures 2a, 2b, and 2c, while Replacement Sheet 2 replaces the original sheet for Figures 2g, 2h, and 2i.

Attachment: Replacement Sheets (2)

Applicant submits that no new matter has been added by the amendments to the drawings.

Allowable Subject Matter

Applicant thanks the Examiner for his indication in the Office Action that claims 9-16 are allowed.

Rejections Under 35 U.S.C. 102(b)

Claims 1-8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. The rejections are traversed for at least the reasons as follow.

Kim et al teach a method for forming a split-gate flash memory. In Kim et al, a first oxidation film and a first conductive layer are etched using an oxidation layer as a mask. See col. 2, lines 35-39 and Fig. 2E of Kim et al. Further, Kim et al teach sequentially depositing a third oxidation film and a third conductive layer over the substrate and thereafter simultaneously etching back a the third oxidation film and the third conductive layer to form a second gate insulating layer and a word line on a sidewall of the oxidation spacer. See col. 2, lines 41-49 of Kim et al.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
>
> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kim et al do not teach or suggest a method for forming a floating gate comprising, *inter alia*, the steps of providing a semiconductor substrate, wherein a gate dielectric layer and a conducting layer are sequentially formed on the semiconductor substrate ... forming a conducting spacer

on a sidewall of a spacer and sequentially removing the exposed conducting layer and the exposed gate dielectric layer, as recited in claim 1.

With reference to Figs. 2F and 2G, the office action states that Kim et al teaches forming a conducting spacer 116 of poly-Si on the sidewall of the first spacer, and removing the exposed conducting layer 114 and gate dielectric layer 113. See page 2 of the office action. However, as clearly shown in the drawings and described in column 2, lines 41-49, Kim et al teach forming a third oxidation film 113 and a third conductive layer 114, and thereafter simultaneously etching back the third oxidation film 113 and the third conductive layer 114 ***to form*** a second gate insulating layer 115 and the word line 116 on the sidewall of the oxidation spacer 106.

Namely, word line 116, which the office action relies upon as the conducting spacer, is ***formed*** by the step of simultaneously removing the oxidation film 113 and the conductive layer 114. Thus, in Kim et al, the "conductive spacer" 116 is formed from the material of the conductive layer 114 by etching.

In contrast, claim 1 recites the steps of, *inter alia*, 1) providing a semiconductor substrate, wherein a gate dielectric layer and a conducting layer are sequentially formed on the semiconductor substrate; 2) forming a conducting spacer on a sidewall of a spacer, the spacer having been formed in previous steps on an exposed portion of conducting layer; and 3) sequentially removing the exposed conducting layer and the exposed gate dielectric layer.

Thus, in the invention recited in claim 1, the conducting spacer is formed ***on*** the conductive layer, as illustrated in the embodiment of the invention shown in Fig. 2g of the application, and the exposed conducting layer and the exposed gate dielectric layer are sequentially removed, as shown in the embodiment of the invention shown in Fig. 2h.

This method and the structure obtained there from cannot be achieved by the method described by Kim et al, in which the conductive spacer is formed ***from*** the conductive layer by etching the conductive layer. Namely, the method of Kim et al will not result in a structure including a conductive spacer formed on a conductive layer.

For at least these reasons, it is Applicant's belief that claim 1 is allowable over the cited reference. Insofar as claims 2-8 and 23 depend from claim 1, it is Applicant's belief that these claims are also in condition for allowance.

New Claim 23

Claim 23 recites a method for forming a floating gate of clam 1, wherein the floating gate consists of the conducting layer and the conducting spacer. As the office action has already indicated that Kim et al does not teach a floating gate consisting of a first conductive layer and a second spacer, it is Applicant's belief that claim 23 is in condition for allowance.

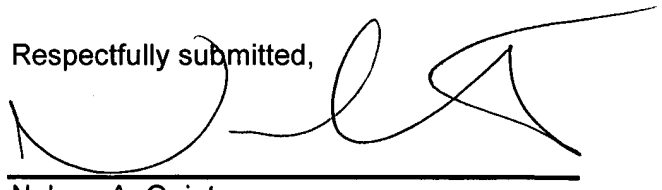
Prior Art in Earlier Application

This application is a divisional application of U.S. Patent Application Serial No. 10/435,416, filed on May 9, 2003. The Examiner is reminded to consider the prior art cited in the parent application. MPEP 609 and 2001.06(b).

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so. The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to Deposit Account No. **502447**. In particular, if this response is not timely filed, then the commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 C.F.R. § 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to Deposit Account No. **502447**.

Respectfully submitted,



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